Journal of Computer and Mathematical Sciences, *Vol.10(5),997-1003 May 2019* *ISSN 0976-5727 (Print)*
(An International Research Journal), *www.compmath-journal.org* *ISSN 2319-8133 (Online)*

Vedic Mathematics Implementation in Multiplier Units

Nitesh Kumar Sharma[1], Deepesh Kumar Gautam[2] and M. R. Khan[3]

[1]Electronics & Communication,
Dr.C.V.Raman University Bilaspur INDIA.
[2]Electronics & Telecommunication,
Govt. Girls Polytechnic Jagdalpur INDIA.
[3]Electronics & Telecommunication, GEC Jagdalpur INDIA.
email:sharma786.nitesh@gmail.com, mrkhan@gecjdp.ac.in, deepeshgautam10@gmail.com.

(Received on: April 25, 2019)

ABSTRACT

A Vedic multiplication algorithm by using Vedic mathematics formula Urdhava Tiryakbhyam method means vertically and cross wise. Vedic mathematics is mainly based on 16 Sutras and was rediscovered in early 20th century. In ancient time in India, people used this Sutra for decimal number multiplications effectively. The same basic concept of Vedic mathematics is applied to multiplication of binary number to make usable in the digital hardware system. The speed of the computation process is increased and the processing time is reduced due to decrease of combinational path delay compared to the traditional method.

Keywords: Vedic maths; tree; multiplier; HDL.

1. INTRODUCTION

Energy consumption is a critical design criterion for today's embedded and mobile systems. Significant effort has already been devoted to improve energy efficiency at various levels, from software, to architecture all the way. The technology is developed with the aim to efficiently serve the computation. The reverse path; evaluating the merit of the algorithms should also be taken. Therefore, it is important to develop computational structures that fit well into the execution model of the processor are optimized and for the current technology.

Vedic Mathematics

The word "Vedas" which literarily means knowledge has derivational meaning as principle and limitless store-house of all knowledge. The word Veda also refers to the sacred

ancient Hindu literature which is divided into four volumes. Vedas are considered to be one of the oldest forms of written records by man. Vedas initially were passed from previous generations to next orally. Later they were transcribed in Sanskrit. A survey of all scripts available of Vedas across different part of India showed no slightest difference in them. Vedas include information from many subjects from religion, medicine, architecture, astronomy, mathematics etc.[1]

A scholar from India Shri Bharati Krishna Tirthaji after careful study of appendix of one of the Vedas –Atharvaveda, reconstructed a mathematical system based on the formulas in it. The main purpose of the system was to use some techniques to solve the lengthy mathematics orally or with minimum space utilization on paper. The system of Vedic mathematics is based on 16 Sutras – formulas and 13 Up-sutras or Corollaries.

1) (Anurupye) Shunyamanyat – If one is in ratio, the other is zero.
1) (Anurupye) Shunyamanyat –The Sutra Anurupye Sunyamanyat says: 'If one is in ratio, the other one is zero'. We use this Sutra in solving a special type of simultaneous simple equations in which the coefficients of 'one' variable are in the same ratio to each other as the independent terms are to each other. In such a context the Sutra says the 'other' variable is zero from which we get two simple equations in the first variable (already considered) and of course give the same value for the variable.
2) Chalana-Kalanabyham – Differences and Similarities. Vedic Mathematics Sri Bharati Krishna Tirthaji mentioned the Sutra 'Chalana - Kalanabhyam' at only two places. The Sutra means 'Sequential motion'
3) Ekadhikina Purvena –. The Sutra (formula) Ekādhikena Pūrvena means: "By one more than the previous one"
4) Ekanyunena Purvena –The Sutra Ekanyunena purvena comes as a Sub-sutra to Nikhilam which gives the meaning 'One less than the previous' or 'One less than the one before'
5) Gunakasamuchyah – The factors of the sum is equal to the sum of the factors.
6) Gunitasamuchyah In connection with factorization of quadratic expressions a sub-Sutra, viz. 'Gunita samuccayah-Samuccaya Gunitah' is useful. It is intended for the purpose of verifying the correctness of obtained answers in multiplications, divisions and factorizations.
7) Nikhilam Navatashcaramam Dashatah –. The formula simply means : "all from 9 and the last from 10" The formula can be very effectively applied in multiplication of numbers, which are nearer to bases like 10, 100, 1000i.e., to the powers of 10 . The procedure of multiplication using the Nikhilam involves minimum number of steps, space, time saving and only mental calculation. The numbers taken can be either less or more than the base considered.
8) Paraavartya Yojayet – Paravartya – Yojayet' means 'transpose and apply'
9) Puranapuranabyham –The Sutra can be taken as Purana - Apuranabhyam which means by the completion or non - completion. Purana is well known in the present system. We can see its application in solving the roots for general form of quadratic equation.
10) Sankalana- vyavakalanabhyam – This Sutra means 'by addition and by subtraction'. It can be applied in solving a special type of simultaneous equations where the x - coefficients and the y - coefficients are found interchanged.

11) Shesanyankena Charamena – The remainders by the last digit.
12) Shunyam Saamyasamuccaye – When the sum is the same that sum is zero. The Sutra Sunyam Samyasamuccaye' says the 'Samuccaya is the same, that Samuccaya is Zero.' i.e., it should be equated to zero. The term 'Samuccaya' has several meanings under different contexts.
13) Sopaantyadvayamantyam – The ultimate and twice the penultimate.
14) Urdhva-tiryakbhyam–Vertically and crosswise. Urdhva–tiryagbhyam is the general formula applicable to all cases of multiplication and also in the division of a large number by another large number.
15)Vyashtisamanstih – Part and Whole.
16)Yaavadunam – Whatever the extent of its deficiency. The meaning of the Sutra is 'whatever the deficiency subtract that deficit from the number and write alongside the square of that deficit'

These methods and ideas can be directly applied to trigonometry, plain and spherical geometry, conics, calculus (both differential and integral), and applied mathematics of various kinds. As mentioned earlier, all these Sutras were reconstructed from ancient Vedic texts early in the last century. Many Sub-sutras were also discovered at the same time, which are not discussed here.

Decimal Multiplication

In Vedic mathematics there are 3 methods to implement multiplication. Out of three there is one generic method which can be applied to all cases whereas other two are for special cases which are simpler to deal with. As the main purpose of Vedic Mathematics is to be able to solve complex calculations by simple techniques which can be done mentally, these Vedic formulas require dealing with very small numbers. The formulas being very short their practical application becomes very simple. Here we will discuss about some of Vedic sutras:

Need of Multiplier Architecture

The core of every microprocessor, digital signal processor (DSP), and data processing application- specific integrated circuit (ASIC) is its data path. It is often the crucial circuit component if die area, power dissipation, and especially operation speed are of concern. At the core of data-path and addressing units in turn are arithmetic units, such as comparators, adders, and multipliers. Finally, the basic operation found in most arithmetic components is the binary addition. Besides of the simple addition of two numbers, adders are also used in more complex operations like multiplication and division. But also simpler operations like incrementing and magnitude comparison base on binary addition.

2. LITERATURE REVIEW

Inexact circuit design is a design philosophy where the conventional constraint of requiring 100% accuracy in circuits is relaxed. Fundamentally, this philosophy adds a fourth dimension of accuracy to the current 3-dimensional circuit design space spanning around power consumption, area and delay. This methodology is applicable in the following two situations.

- The first situation is where the circuits are inherently "unreliable" and "probabilistic". Increasing parameter variations, noise susceptibility and decreasing process sizes are causing CMOS devices to be non-deterministic. To address these issues and precisely model the effect of these probabilistic circuit elements, the metric of accuracy needs to be introduced into the entire circuit design framework.
- The second situation is where the circuits themselves are not probabilistic in nature but are deterministic, but the application does not demand 100% accuracy. In such cases, relaxing the very rigid constraint of accuracy can be used to decrease energy consumption which is one of the leading challenges in current day circuit design[2,18]. There are many researchers provide a many types of Accurate Vedic & Multipliers.

Tree Multiplier

The tree multiplier reduces the time for the accumulation of partial products by adding all of them in parallel, whereas the array multiplier adds each partial product in series. The tree multiplier commonly uses CSAs to accumulate the partial products.

An Efficient High Speed Wallace Tree Multiplier

In this paper author use the existing Wallace tree approach but here they are using carry select adders which will reduce the latency of previous existing approach. A Wallace tree multiplier is an improved version of tree based multiplier architecture. It uses carry save addition algorithm to reduce the latency. This paper aims at further reduction of the latency and power consumption of the Wallace tree multiplier. This is accomplished by the use of 4:2, 5:2 compressors and a proposed carry select adder.

Comparative Analysis for Hardware Circuit Architecture of Wallace Tree Multiplier

The reduction of partial products using full adders as carry-save adders (also called 3:2 counters) became generally known as the Wallace Tree". According to this paper author used existing Wallace tree method but the use small size full adder which will reduce the hardware consumption. This architecture reduces the partial products at a rate of log 3 2 (N 2). Figure shows an example of tree reduction for an 8*8-bit partial product tree. The ovals around the dots represent either a full adder (for three circled dots) or a half adder (for two circled dots). This tree is reduced to two rows for a carry-propagate adder after four stages. There are many ways to reduce this tree with CSAs, and this example is just one of them.

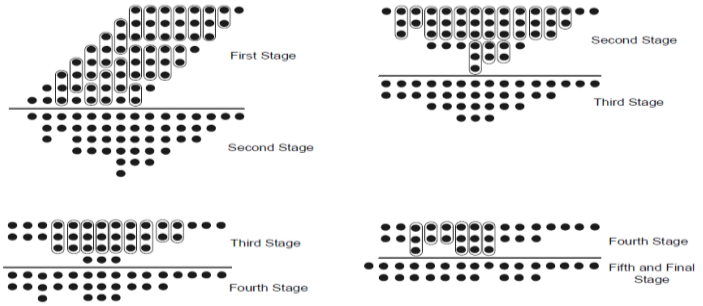


Figure.1 Wallace Tree Multiplier

Methodology

Urdhva tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and crosswise". The conventional methods already know to us will require 16 multiplications and 15 additions. An alternative method of multiplication using Urdhva tiryakbhyam Sutra is shown in below Fig.1 The numbers to be multiplied are written on two consecutive sides of the square as shown in the figure. The square is divided into rows and columns where each row/column corresponds to one of the digit of either a multiplier or a multiplicand. Thus, each digit of the multiplier has a small box common to a digit of the multiplicand. These small boxes are partitioned into two halves by the crosswise lines. Each digit of the multiplier is then independently multiplied with every digit of the multiplicand and the two-digit product is written in the common box. All the digits lying on a crosswise dotted line are added to the previous carry. The least significant digit of the obtained number acts as the result digit and the rest as the carry for the next step. Carry for the first step (i.e., the dotted line on the extreme right side) is taken to be zero.

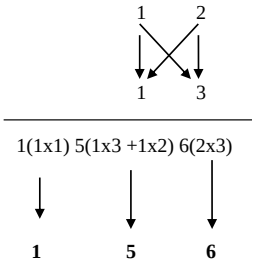


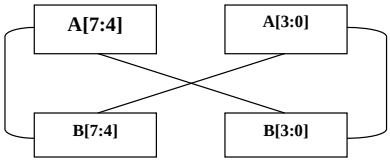
Figure.2 Simple Urdhva Tiryakbhyam Multiplication

Urdhva Tiryakbhyam Multiplication for 4 bit Multiplier using two Binary Numbers

				X_3	X_2	X_1	X_0	Multiplicand
				Y_3	Y_2	Y_1	Y_0	Multiplier
H	G	F	E	D	C	B	A	
P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0	Product

Figure.3 Algorithm for 4 x 4 bit Vedic multiplier Using Urdhva Tiryakbhyam (Vertically and crosswise) for two binary numbers.

Urdhva Tiryakbhyam Multiplication for 8 bit Multiplier using two Binary Numbers



Step1: P[7:0] = A[3:0]xB[3:0]
Step2: P[7:0] = A[7:4]xB[3:0]
Step3: P[7:0] = A[3:0]xB[7:4]
Step4: P[7:0] = A[7:4] xB[7:4]

Figure.4 Algorithm for 8 X 8 Bit Multiplication Using Urdhva Triyakbhyam (Vertically and crosswise) for two Binary numbers

EXPECTED OUTCOME

The goal of this project is to design and implement a multiplier unit which based on Vedic Mathematics concept. In this work, the main focus is on performance and accuracy, but we do provide some numbers for the arithmetic units relating to speed and power. This is to provide an estimate of the amount and power consumed by the units we choose to implement. The priorities of this project, in order of importance, are: Area or speed balance, avoid complexity of circuits and Design time.

REFERENCES

1. Garcia, Oscar N., Harvey Glass, and Stanley C. Haimes. "An approximate and empirical study of the distribution of adder inputs and maximum carry length propagation." *Computer Arithmetic (ARITH), 1978 IEEE 4th Symposium on. IEEE*, (1978).
2. Marr, David, and Ellen Hildreth. "Theory of edge detection." *Proceedings of the Royal Society of London B: Biological Sciences* 207.1167: 187-217 (1980).
3. Canny, John. "A computational approach to edge detection." *Pattern Analysis and Machine Intelligence,IEEE Transactions* on 6: 679-698 (1986).
4. Unser, Michael, and Murray Eden. "Multiresolution feature extraction and selection for texture segmentation." *Pattern Analysis and Machine Intelligence, IEEE Transactions on* 11.7: 717-728 (1989).
5. Borkar, Shekhar. "Design challenges of technology scaling." *Micro, IEEE* 19.4: 23-29 (1999).
6. Reinhard, Erik, *et al*. "Photographic tone reproduction for digital images." *ACM Transactions on Graphics (TOG)*. Vol. 21. No. 3. ACM, (2002).
7. ZhouWang; Bovik, A.C.; Sheikh, H.R.; Simoncelli, E.P., "Image quality assessment: from error visibility to structural similarity," *Image Processing, IEEE Transactions* on , vol.13, no.4, pp.600,612, 10.1109/TIP.2003.819861 (April 2004).
8. Tiwari, Honey Durga, *et al*. "Multiplier design based on ancient Indian Vedic Mathematics." SoC Design Conference, 2008. ISOCC'08. *International*. Vol. 2. *IEEE,* (2008).
9. Lee, Kyoungwoo, *et al*. "Error-exploiting video encoder to extend energy/qos tradeoffs for mobile embedded systems." Distributed Embedded Systems: Design, Middleware and Resources. Springer US, 23-34 (2008).
10. Palem, Krishna V., *et al*. "Sustaining moore's law in embedded computing through probabilistic and approximate design: retrospects and prospects."Proceedings of the 2009 international conference on Compilers, architecture, and synthesis for embedded systems. ACM, (2009).
11. Guo, Zhengyang, Wenbo Xu, and Zhilei Chai. "Image edge detection based on FPGA." Distributed Computing and Applications to Business Engineering and Science (DCABES), 2010 *Ninth International Symposium on. IEEE,* (2010).
12. Lomte, Rashmi K., and P. C. Bhaskar. "High Speed Convolution and Deconvolution Using Urdhva Triyagbhyam." *VLSI (ISVLSI), 2011 IEEE Computer Society Annual Symposium on. IEEE*, (2011).

13. Cho, Hyungmin, Larkhoon Leem, and Subhasish Mitra. "ERSA: Error resilient system architecture for probabilistic applications." Computer-Aided Design of Integrated Circuits and Systems, *IEEE Transactions* on 31.4: 546-558 (2012).
14. Saokar, Sandesh S., R. M. Banakar, and Saroja Siddamal. "High speed signed multiplier for digital signal processing applications." Signal Processing, Computing and Control (ISPCC), 2012 *IEEE International Conference on. IEEE*, (2012).
15. Stine, James E. Digital computer arithmetic datapath design using verilog HDL. *Springer Science & Business Media*, (2012).
16. Sureka, N., R. Porselvi, and K. Kumuthapriya. "An efficient high speed Wallace tree Multiplier." *Information Communication and Embedded Systems (ICICES), 2013 International Conference on. IEEE*, (2013).
17. Itawadiya, Akhalesh K., et al. "Design a DSP operations using vedic mathematics." *Communications and Signal Processing (ICCSP), 2013 International Conference on. IEEE*, (2013).
18. Kirubaveni, S. "Performance evaluation of FFT processor using conventional and Vedic algorithm." Emerging Trends in Computing,Communication and Nanotechnology *(ICE-CCN), 2013 International Conference on. IEEE,* (2013).
19. Gandhi, Dhaval R., and Nehal N. Shah. "Comparative analysis for hardware circuit architecture of Wallace tree multiplier." *Intelligent Systems and Signal Processing (ISSP), 2013 International Conference on. IEEE,* (2013).
20. Garima Rawat, Khyati Rathore, Siddharth Goyal, Shefali Kala and Poornima Mittal "Design and Analysis of ALU: Vedic Mathematics Approach" *International Conference on Computing, Communication and Automation (ICCCA 2015)*. IEEE (2015).
21. Dravik KishorBhai Kahar and Harsh Mehta "High Speed Vedic Multiplier Used Vedic Mathematics" *International Conference on Intelligent Computing and Control Systems ICICCS 2017. IEEE* (2017).
22. Books: Vedic Ganit by Ashish Sipai.